FORM PTO-1390
(REV 12-29-99)

U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER

JC10 Rec'd PCT/PTO 2 1 MAR 2001
MOT-D2194

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1 5)

09/787601

INTERNATIONAL APPLICATION NO. PCT/US99/21874	INTERNATIONAL FILING DATE 21 September 1999	PRIORITY DATE CLAIMED 21 September 1998

TITLE OF INVENTION   APPARATUS AND METHOD FOR MERGING VERTICAL BLANKING INTERVALS

APPLICANT(S) FOR DO/EO/US Anthony Cucinotta

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. [ ] This is a **SECOND or SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. [ ] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))

    a. [X] is transmitted herewith (required only if not transmitted by the International Bureau).

    b. [X] has been transmitted by the International Bureau.

    c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).

6. [ ] A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. [X] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))

    a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).

    b. [ ] have been transmitted by the International Bureau.

    c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.

    d. [X] have not been made and will not be made.

8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. [ ] A FIRST preliminary amendment.

    [ ] A SECOND or SUBSEQUENT preliminary amendment.

14. [ ] A substitute specification.

15. [ ] A change of power of attorney and/or address letter.

16. [X] Other items or information:
International Publication with Search Report;
International Preliminary Examination Report;
Written Opinion; and
Reply to Written Opinion

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/787601	PCT/US99/21874	MOT-D2194

17. [X] The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

	CALCULATIONS	PTO USE ONLY

Neither international preliminary examination fee (37 CFR 1.482)
nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO
and International Search Report not prepared by the EPO or JPO · · · · · · · · · $1,000.00

International preliminary examination fee (37 CFR 1.482) not paid to
USPTO but International Search Report prepared by the EPO or JPO · · · · · · · $860.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but
international search fee (37 CFR 1.445(a)(2)) paid to USPTO · · · · · · · · · · $710.00

International preliminary examination fee paid to USPTO (37 CFR 1.482)
but all claims did not satisfy provisions of PCT Article 33(1)-(4) · · · · · · · · · · $690.00

International preliminary examination fee paid to USPTO (37 CFR 1.482)
and all claims satisfied provisions of PCT Article 33(1)-(4) · · · · · · · · · · · · · · · $100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 [X] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	24 - 20 =	4	X $18.00	$ 72.00	
Independent claims	3 - 3 =	0	X $80.00	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $260.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 1062.00	
Reduction of 1/2 for filing by small entity, if applicable. A Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$ 1062.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 1062.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
TOTAL FEES ENCLOSED =				$ 1062.00	
				Amount to be refunded:	$
				charged:	$

a. [X] A check in the amount of $ 1062.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 22-0493 . A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Volpe and Koenig, P.C.
Suite 400, One Penn Center
1617 John F. Kennedy Boulevard
Philadelphia, PA 19103

SIGNATURE

Gerald B. Halt, Jr., Esquire

NAME

37,633

REGISTRATION NUMBER

APPARATUS AND METHOD FOR
MERGING VERTICAL BLANKING INTERVALS

BACKGROUND

This invention is related to cable television (CATV) and wireless transmission

5   systems. More particularly, the invention is related to an apparatus for merging

selected lines of at least two vertical blanking intervals (VBIs) for transmission over

the RF band which is typically reserved for a single VBI.

With the increasing array of services from CATV and wireless network

operators, it has become imperative for operators to offer more services in the same

10   amount of RF transmission bandwidth. Moreover, wireless pay television systems,

whether MMDS or conventional VHF/UHF television, are generally constrained to

far fewer channels than the conventional CATV systems with which they compete.

The challenge is offering more channels to subscribers within the spectrum

constraints imposed by government regulations.

15   For a typical television program, since the video portion of the program

occupies most of the available 6 MHz on an NTSC television channel, much of the

research toward maximizing the amount of bandwidth has been traditionally devoted

towards compressing and minimizing the amount of bandwidth the video

information occupies. Accordingly there exists a need for providing more channel

20   capacity within the same amount of transmission bandwidth while maintaining the

quality of the transmitted data.

Ancillary information services are typically transmitted using existing

television broadcast channels. The ancillary information is transmitted in the VBI

-2-

and decoded at a television in order to display the ancillary information along with the television picture. Ancillary information typically includes text, for example closed captioning or related program information. Since the ancillary information transmitted along the VBI does not typically utilize the entire bandwidth assigned to

5   the VBI, it is desirable to merge several VBIs into the bandwidth allotted for a single VBI in order to minimize the overall bandwidth required for the television transmission.

United Kingdom Patent Application No. GB 2286321A discloses a method for data distribution comprising storing packets of data in a random access memory,

10   storing transmission characteristics for each packet, reading the characteristics and transmitting each packet to an audience in accordance with the frequency and timing parameters set forth in the packets' particular transmission characteristics. However, this system does not have the capability of merging the information from several VBIs into the bandwidth allotted for a single VBI.

15

SUMMARY

It is therefore an object of the invention to provide a method and apparatus for merging VBIs into the bandwidth allotted for a single VBI.

This and other objects have been achieved by providing a method and an

20   apparatus for merging VBIs. The VBIs are merged by sequentially writing selected VBIs of a field to a first memory, then writing selected VBIs of a second field to a second memory while reading VBIs from the first memory in a desired sequence.

-3-

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of the merging system according to the present invention; and

Figure 2 is a diagram VBIs from two services merged into a single VBI.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention will now be described in greater detail with reference to the drawings, wherein like numerals represent like elements throughout. The system **10** shown in **Figure 1** for merging VBIs is divided into two symmetric halves **20, 60**. The first half **20** is connected to a first service which will be referred to as service A while the second half **60** is connected to a second service which will be referred to as service B. A field programable gate array (FPGA) **40** is connected to a microprocessor (not shown) and controls both halves **20, 60**. The preferred FPGA **40** for this system is a QuickLogic QL3025-2 PQ208C. It should be understood however that other commercially available field programmable gate arrays or other control circuits having similar functionality may be utilized as a substitute for this component. The FPGA **40** is preferably controlled by a microprocessor on a Zilog Z8S180 circuit card. It should also be understood that other commercially available microprocessors serving similar FPGA control functions may be utilized as a substitute for this component.

The FPGA **40** is connected to an input multiplexer **24** which receives input data from service A at port **22**. The input multiplexer **24** has a first output **41**

connected to number 1 data bus and a second output **42** connected to number 2 data bus. Both number 1 data bus and number 2 data bus are bidirectional to allow data flow in both directions. Memory **26** is connected to number 1 data bus at **46** and is controlled by the FPGA **40**. It should be understood that while the memories **26** and

5   **30** are shown as static RAM, other suitable memory devices may be utilized for this application. An address bus **45** extends from the memory **26** to a first control multiplexer **28**. The first control multiplexer **28** has a first input **52** connected to the FPGA **40** and an output port **54** also connected to the FPGA **40**. Input **52** is connected to a corresponding input on control multiplexers **62, 63** in the second half

10   **60**. Likewise, output port **54** is also connected to corresponding outputs on control multiplexers **62, 63** in the second half **60**. A directional signal from the FPGA **40** is connected to the control multiplexer **28** at I/O select port **44**. Likewise, a second directional signal from the FPGA **40** is connected to the control multiplexer **32** at I/O select port **43**.

15   The number 1 data bus also extends to an output multiplexer **34** at port **36**. The output multiplexer is connected to the number 2 data bus at port **38**. A second memory **30** is connected to the number 2 data bus at port **50** and to an address bus **49** at port **48**. The address bus **49** extends to a second control multiplexer **32** having an I/O select port **56** being connected to the input **52** of the first control multiplexer

20   **28**. An output port **58** is connected to the output port **54** of the first control multiplexer **28**. Both ports **56** and **58** are also connected to the FPGA **40** and to corresponding control multiplexers **62, 63** in the second half **60**. An output data bus

59 extends from the output multiplexer **34** and is coupled to a complimentary output multiplexer **64** of the second half **60**.

Operation of the system **10** will be described in greater detail with reference to **Figures 1** and **2**. Turning first to **Figure 2**, it should be understood that a pair of

5   services each containing a series of VBI information stored along selected lines of a picture field are to be merged into a single VBI. For example, **Figure 2** shows a sample merged VBI. It can be seen that selected lines from service A and selected lines from service B are assembled into selected locations in the merged VBI. It should also be understood that, while only part of the lines displayed for service A

10   and part of the lines for service B have been selected for the merged VBI, the merged VBI could be sized accordingly to receive all the selected lines of service A and all the selected lines of service B as long as the merged VBI does not exceed a maximum size limitation of a given television picture field. Assume, for example, that the desired information to be transmitted from service A appears on lines 10-21

15   of service A. Assume also, that the desired VBI information of service B appears at lines 10-21. The merged VBI can contain some of the lines from each service as shown in **Figure 2** or it may contain all of the lines 10-21 from each service. This control is achieved by programming the FPGA **40** using a microprocessor (not shown). Those reasonably skilled in the art would appreciate that while lines 10-21

20   have been selected in these services for transmitting data along the VBI, other lines could be selected for transmitting the same data.

Referring back to **Figure 1**, service A is sampled at a desirable sample rate,

for example this system utilizes 909 samples per video line, however it should be

understood that other sample rates may be selected based upon design requirements

or preferences. Service A sample data **22** is fed into the input multiplexer **24**. The

5   FPGA **40** controls the input multiplexer **22** to send the sample data either to port **41**

along number 1 data bus or port **42** along number 2 data bus. The FPGA **40** controls

each memory **26**, **30** so that, while memory **26** is receiving data from the input

multiplexer **22** along number 1 data bus (write cycle), memory **30** is being read from

port **50** along the number 2 data bus (read cycle) and vice versa. Therefore, VBI

10   lines corresponding to a given field and sampled at a rate of 909 samples per line are

written into memory **26** while a series of lines from the previous field having been

stored in a similar fashion are being read from the memory **30**.

Each of the memories **26**, **30** are controlled through a respective control

multiplexer **28**, **32**. The FPGA **40** sends input addresses along the input address bus

15   through input **52** and address bus **45** to the memory **26** to indicate where each

consecutive sample for the series of VBI lines is to be stored. These addresses are

preferably sequential addresses, however it should be understood that the FPGA **40**

may be programmed to control the memory **26** so that samples are stored in a non-

sequential manner. Data is read from the memory **26** in the following cycle along

20   number 1 data bus. Data is read from the memory **26** according to addresses sent by

the FPGA **40** along the output address bus to output port **54**. The data is read out of

the memory in a non-sequential order as directed by addresses sent from the FPGA

40 through output port 54 of the control multiplexer 28. For example, as shown in Figure 2, data written in from line 18 of service B could be read out at line 12 in the merged VBI. The FPGA 40 could optionally be programmed to send addresses to the memory 26 such that data is read out sequentially. The data in the form of

5   sampled VBIs is read along number 1 data bus into port 36 of the output multiplexer 34 and on to the output data bus 59. It should be understood that during a first cycle, the number 2 data bus has data flowing from the input multiplexer 24 into the memory 30 and there is no data flowing into port 38 of the output multiplexer 34. During the next cycle, data is read from the memory 30. The output data bus

10   therefore receives non-sequential VBI line data corresponding to a first field from memory 26 and then receives non-sequential VBI data from a second field from memory 30. It should be understood however that the FPGA 40 could be programmed to read data out in any order including a sequential order. This process is duplicated for service B in system half 60. The processes are synchronized so that

15   when memory 26 is in a read cycle, memory 66 is also in a read cycle. Accordingly, when memory 30 is in a read cycle, memory 68 is also in a read cycle. The same applies to memories 26 and 66. Write cycles are similarly synchronized. The output data bus 59 therefore receives some line samples from output multiplexer 34 and some line samples from output multiplexer 64 to create the merged VBI shown in

20   Figure 2. The FPGA 40 controls the selection of lines from each service. Therefore, for each line of the merged VBI, (Figure 1) the FPGA 40 selects the service and line number from data previously stored in the memories.

An advantage of this invention is that several services VBIs may be transmitted in a single VBI thus reducing the bandwidth necessary for transmission.

It will be understood by those reasonably skilled in the art that minor variations of the embodiment presented here are intended to be within the scope of the invention. For example, where reference is made to sampling or digitizing data, it should be appreciated that similar analog methods could be substituted. Other such minor variations are intended to be within the scope of the invention which is intended to be limited only by the appended claims.

5

SCANNED, #——

-9-

What is claimed is:

1. A method for merging vertical blanking intervals comprising:

storing a plurality of lines of data from a first service in a first memory (26) during a first write cycle;

storing a plurality of lines of data from a second service in a third memory (66) during the first write cycle;

storing a second plurality of lines of data from the first service in a second memory (30) during a second write cycle;

storing a second plurality of lines of data from the second service in a fourth memory (68) during the second write cycle;

reading selected lines of the data in the second and fourth memories (30), (68) during the first write cycle; and

reading selected lines of the data in the first and third memories (26), (66) during the second write cycle.

2. The method of claim 1 wherein the memories (26), (30), (66), (68) are controlled by a controller (40).

3. The method of claim 2 wherein the controller (40) sends memory addresses to the memories (26), (30), (66), (68) during the write cycles to direct the data into selected memory locations.

AMENDED SHEET

-10-

4. The method of claim 3 wherein data is selected and read from locations in each memory (26), (30), (66), (68) according to addresses sent from the controller (40).

5. An apparatus for merging video data comprising:

a controller (40);

first (26), second (30), third (66), and fourth (68) memories, responsive to said controller (40);

an input address bus (45), (49) connected between the controller (40) and the memories (26), (30), (66), (68);

an output address bus connected between the controller (40) and the memories (26), (30), (66), (68);

a first service input (22) connected to the first (26) and second (30) memories; and

a second service input (65) connected to the third (66) and fourth (68) memories; and an output bus (59) connected to the first (26), second (30), third (66), and fourth (63) memories.

6. The apparatus according to claim 5 further comprising a plurality of control multiplexers (28), (32), (62), (63) operatively connected to the controller (40), each for controlling a respective one of the memories (26), (30), (66), (68).

-11-

7. The apparatus according to claim 5 wherein the controller (40) comprises a field programmable gate array.

8. The apparatus according to claim 5 further comprising an output data bus (59) connected to each of the memories (26), (30), (66), (68).

9. The apparatus according to claim 8 further comprising a first output multiplexer (34) operatively connected between the first (26) and second (30) memories.

10. The apparatus according to claim 9 further comprising a second output multiplexer (64) operatively connected to the first output multiplexer (34) and between the third (66) and fourth (68) memories.

11. The apparatus according to claim 8 further comprising a first input multiplexer (24) for directing data into the first (26) and second (30) memories.

12. The apparatus according to claim 11 further comprising a second input multiplexer for directing data into the third (66) and fourth (68) memories.

13. The apparatus of claim 5 wherein said controller (40) stores data in the first (26) and third (66) memories while selectively reading data from the second (30)

-12-

and fourth (68) memories during a first cycle, and stores data in the second (30) and

fourth (68) memories while selectively reading data from the first (26) and third (66)

5   memories during a second cycle.

14.   The apparatus according to claim 13 further comprising a plurality of

control multiplexers (28), (32), (62), (63) operatively connected to each other and

each being connected to a respective one of the memories (26), (30), (66), (68).

15.   The apparatus according to claim 14 wherein said plurality of control

multiplexers (28), (32), (62), (63) controls data flow in to and out of its respective

memory (26), (30), (66), (68).

16.   The apparatus according to claim 15 wherein said first output multiplexer

(34) directs data out of the first (26) and second (30) memories to a common data

bus (59).

17.   The apparatus according to claim 16 wherein said second output

multiplexer (64) directs data out of the third (66) and fourth (68) memories to the
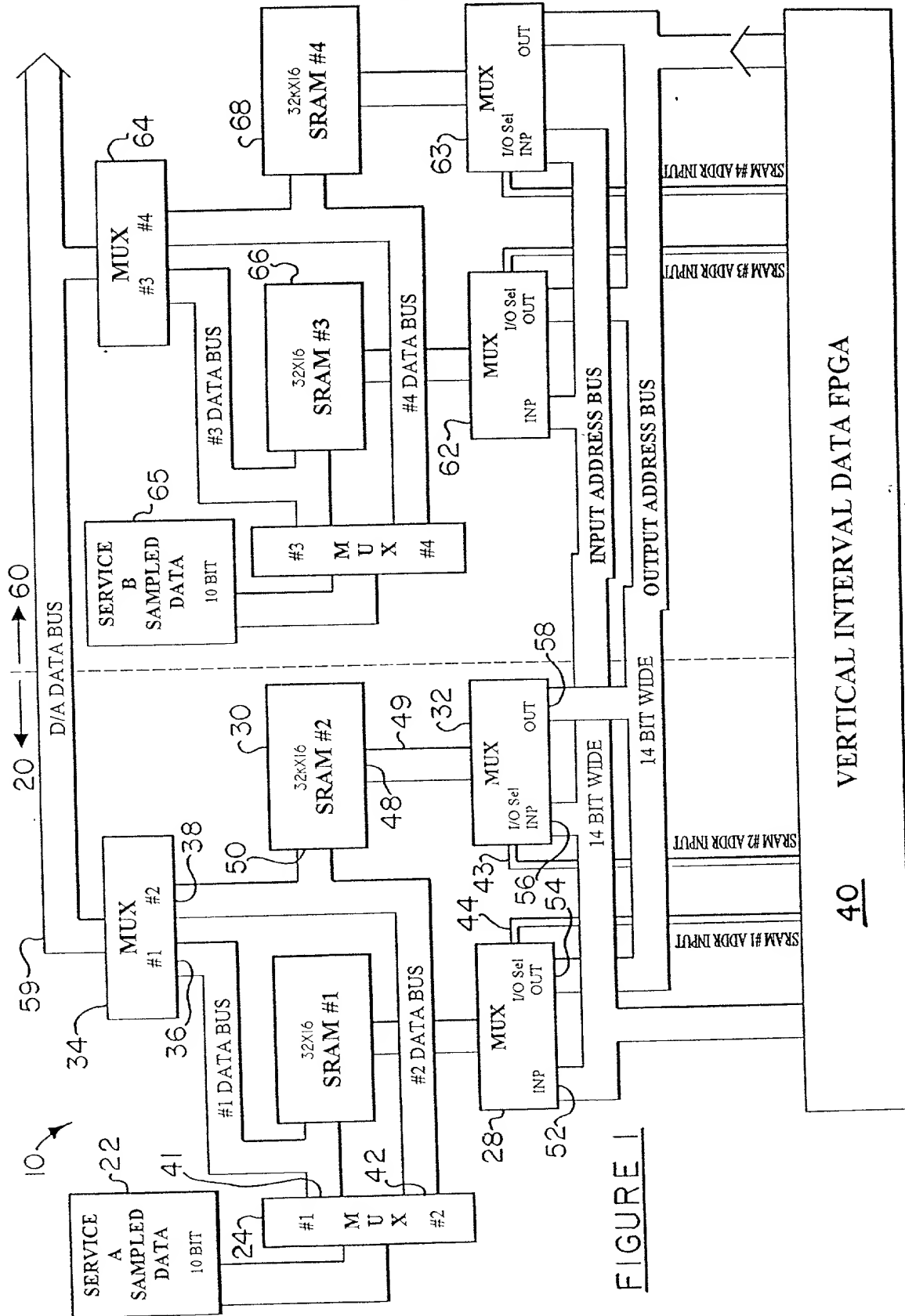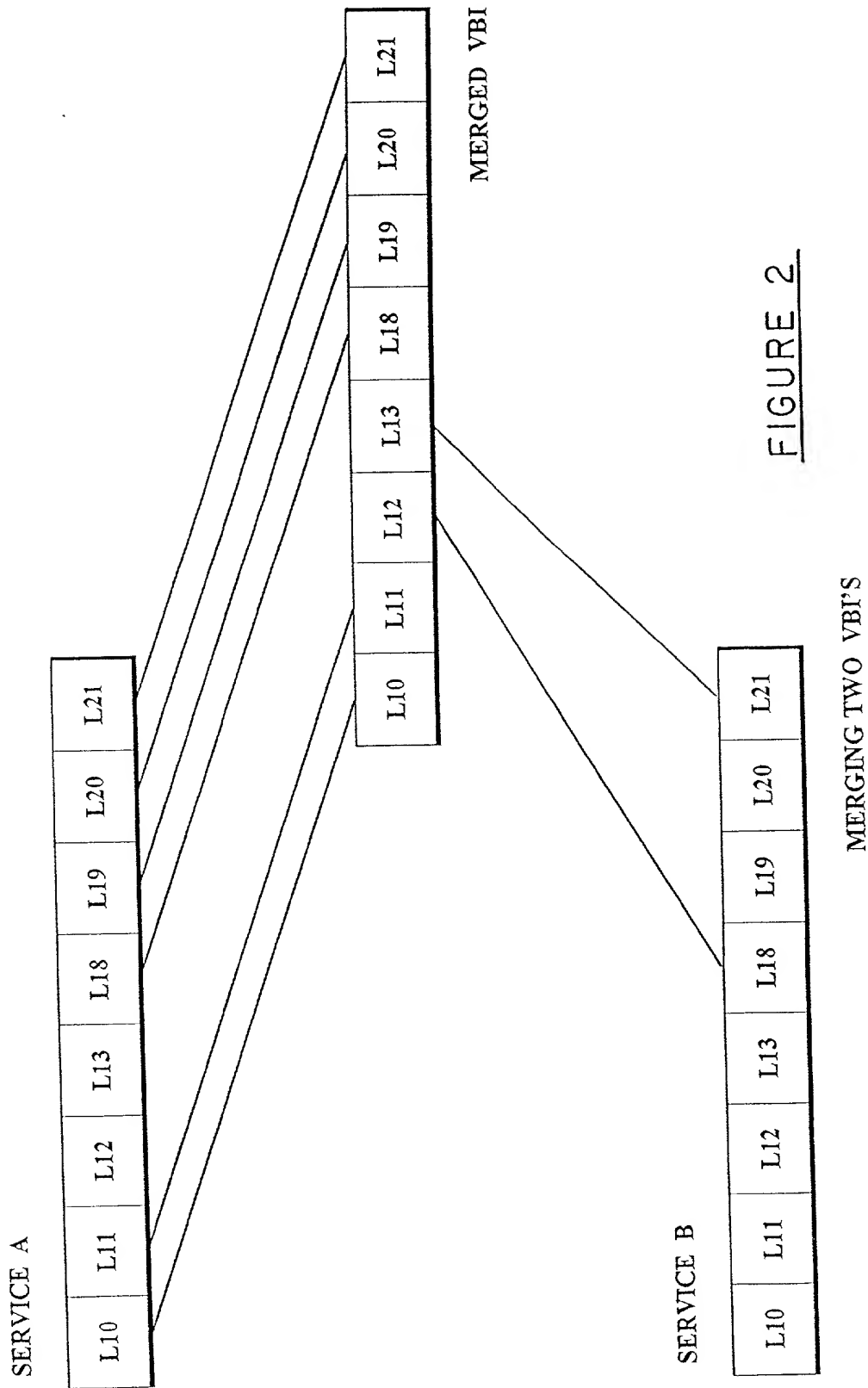
common data bus (59).

AMENDED SHEET

FIGURE 1

09/787601

SERVICE A

L10	L11	L12	L13	L18	L19	L20	L21

MERGED VBI

L10	L11	L12	L13	L18	L19	L20	L21

SERVICE B

L10	L11	L12	L13	L18	L19	L20	L21

MERGING TWO VBI'S

FIGURE 2

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)	**Attorney Docket Number**	MOT-D2194
	First Named Inventor	Anthony Cucinotta
	COMPLETE IF KNOWN	
	Application Number	09/787,601
	Filing Date	Not Yet Known
☐ Declaration Submitted with Initial Filing **OR** ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)	Group Art Unit	Not Yet Known
	Examiner Name	Not Yet Known

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

APPARATUS AND METHOD FOR MERGING VERTICAL BLANKING INTERVALS

the specification of which
☐ is attached hereto *(Title of the Invention)*
OR
☒ was filed on (MM/DD/YYYY) 09/21/1999 as United States Application Number or PCT International

Application Number PCT/US99/21874 and was amended on (MM/DD/YYYY) [   ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	
60/101,181	09/21/1998	☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

Please type a plus sign (+) inside this box → ☐ +

DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)
PCT/US99/21874	09/21/1999	

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☒ Customer Number .24375.   →   *Place Customer Number Bar Code Label here*
OR
☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number
Namely, the Attorneys of Volpe and Koenig, P.C.			

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☒ Customer Number or Bar Code Label   24375   OR ☐ Correspondence address below

Name	VOLPE AND KOENIG, P.C. DEPT MOT
Address	
Address	

City		State		ZIP	
Country		Telephone		Fax	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor:	☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Anthony	Cucinotta

Inventor's Signature	*[signature]*			Date	June 25, 2001
Residence: City	Flower Mound	State	TX	Country	USA	Citizenship	USA
Post Office Address	1525 Latigo Hills Trail				
Post Office Address					
City	Flower Mound	State	TX	ZIP	75022	Country	USA

☐ Additional inventors are being named on the _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto